

**IN THE CLAIMS**

1. (Currently Amended) A process of treating a semiconductor structure comprising:  
providing a substrate;  
providing a gate stack comprising a gate dielectric layer disposed over the substrate; a polysilicon layer disposed over the gate dielectric layer; a barrier layer disposed over the gate dielectric layer, and a metal film disposed over the polysilicon layer;  
patterning the metal film, barrier layer and polysilicon layer to form a patterned gate stack;  
and  
oxidizing the ~~polysilicon layer~~ patterned gate stack under conditions that reduce redeposition on the substrate and on the gate stack of a volatilized portion of the metal film.
2. (Withdrawn) The process according to claim 1, wherein the conditions that reduce redeposition include using a fluorine-containing composition disposed in a layer over the gate stack.
3. (Withdrawn) The process according to claim 1, wherein the conditions that reduce redeposition include using fluorine disposed in a dielectric cap layer over the metal film.
4. (Withdrawn) The process according to claim 1, wherein the conditions that reduce redeposition include using fluorine disposed in a dielectric cap layer disposed over the metal film, wherein the dielectric cap layer contains fluorine in a range from about 0.1% to about 30%.
5. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using a fluorine-containing composition that is metered to the substrate and gate stack in gaseous form.
6. (Original) The process according to claim 1, wherein the conditions that reduce redeposition include using  $\text{NF}_3$  gas that is metered to the substrate and gate stack.

7. (Withdrawn) The process according to claim 1, wherein the conditions that reduce redeposition include using a fluorine-containing composition disposed in a layer in the gate stack, and a fluorine-containing composition that is metered to the substrate and gate stack in gaseous form.
8. (Withdrawn) The process according to claim 1, wherein the conditions that reduce redeposition include using fluorine disposed in a dielectric nitride cap layer over the metal film, wherein the dielectric nitride cap layer contains fluorine in a range from about 0.1% to about 30%.
9. (Original) A process comprising:  
forming a metal film over a structure; and  
thermally processing the structure in the presence of a first composition such that the metal is more likely to combine with at least a portion of the first composition than with the structure.
10. (Original) The process according to claim 9, wherein the structure comprises oxide surfaces, and wherein the conditions are sufficient to cause the first composition to resist etching the oxide surfaces.
11. (Original) The process according to claim 9, wherein the first composition comprises  $\text{NF}_3$ .
12. (Original) The process according to claim 9, wherein the first composition comprises  $\text{NF}_3$  in a gaseous state.
13. (Withdrawn) The process according to claim 9, wherein the first composition comprises  $\text{NF}_3$  in a solid state.

14. (Original) The process according to claim 9, wherein the first composition comprises a halogen-containing composition.
15. (Original) The process according to claim 9, wherein the first composition comprises a halogen-containing composition in a gaseous state.
16. (Withdrawn) The process according to claim 9, wherein the first composition comprises a halogen-containing composition in a solid state.
17. (Previously Presented) The process according to claim 9, further comprising:  
forming a spacer layer over the structure; and  
etching the spacer layer.
18. (Previously Presented) A process comprising:  
forming a doped polysilicon layer over a substrate;  
forming a barrier layer over the doped polysilicon layer;  
forming a metal film over the barrier layer;  
forming a nitride layer over the metal film to form a gate stack disposed on a substrate;  
and  
thermally processing the gate stack in the presence of a fluorine-containing composition under conditions sufficient to cause the metal film more likely to combine with the fluorine-containing composition than with the gate stack or the substrate.
19. (Original) The process according to claim 18, wherein the barrier layer includes a metal nitride barrier layer.
20. (Original) The process according to claim 18, wherein the gate stack and the substrate include oxide surfaces, and wherein the conditions are sufficient to cause the fluorine-containing composition to resist etching the oxide surfaces.

21. (Original) The process according to claim 18, wherein the fluorine-containing composition comprises  $\text{NF}_3$ .
22. (Original) The process according to claim 18, wherein the metal film is selected from Al, Cu, Ag, Au, Ti, Zr, Hf, Ni, Co, Pd, Pt, V, Ta, Nb, Cr, Mo, W, Sc, Yt, La, Ce, Rh, Os, Ir, and combinations thereof.
23. (Withdrawn) The process according to claim 18, wherein the fluorine-containing composition comprises  $\text{NF}_3$  in a solid state.
24. (Withdrawn) The process according to claim 18, wherein the fluorine-containing composition comprises the nitride layer.
25. (Withdrawn) The process according to claim 18, wherein the fluorine-containing composition comprises the metal film.
26. (Withdrawn) The process according to claim 18, wherein the fluorine-containing composition comprises the metal nitride barrier layer.
27. (Withdrawn) A process of forming a gate stack comprising:  
providing a substrate;  
forming a gate dielectric layer over the substrate;  
depositing a polysilicon layer over the gate dielectric layer;  
forming a metal film above the polysilicon layer;  
forming a cap layer over metal film;  
etching a gate stack through the cap layer, the metal film, and the polysilicon layer, under conditions that reduce redeposition on the substrate of a volatilized portion of the metal film; and  
wherein at least one process of depositing a polysilicon layer, forming a metal film, and forming a cap layer is carried out in the presence of a metal-reducing composition.

28. (Withdrawn) The process according to claim 27, wherein the conditions that reduce redeposition include using a halogen-containing composition that is metered to the substrate in gaseous form.
29. (Withdrawn) The process according to claim 27, wherein the conditions that reduce redeposition include using  $\text{NF}_3$  gas that is metered to the substrate.
30. (Withdrawn) The process according to claim 27 following etching a gate stack, further comprising:  
oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film.
31. (Original) The process according to claim 27 following etching a gate stack, further comprising:  
oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film; and  
forming a spacer layer over the gate stack under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film.
32. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using a halogen-containing composition that is metered to the substrate and gate stack in gaseous form.
33. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using  $\text{NF}_3$  gas that is metered to the substrate and gate stack.
34. (Withdrawn) The process according to claim 31, wherein the conditions that reduce redeposition include using a halogen-containing composition disposed in a layer or the film in the gate stack, and a halogen-containing composition that is metered to the substrate and gate stack in gaseous form.

35. (Withdrawn) The process according to claim 31, wherein the conditions that reduce redeposition include using fluorine disposed in the cap layer over the metal film.

36. (Withdrawn) A process of making a computer system, comprising:  
forming a processor;  
forming a memory system coupled to the processor; and  
forming an input/output circuit coupled to the processor and the memory system; wherein at least one of forming a processor and forming an input/output circuit include:  
providing a substrate;  
forming a gate dielectric layer over the substrate;  
depositing a polysilicon layer over the gate dielectric layer;  
forming a metal film above the polysilicon layer;  
forming a cap layer over metal film;  
etching a gate stack through the cap layer, the metal film, and the polysilicon layer, under conditions that reduce redeposition on the substrate of a volatilized portion of the metal film; and  
wherein at least one process of depositing a polysilicon layer, forming a metal film, and forming a cap layer is carried out in the presence of a metal-reducing composition.

37. (Withdrawn) The process according to claim 36, wherein the memory system is disposed in a host selected from a memory module, a device driver, a power module, a communication modem, a processor module, and an application specific integrated circuit.

38-66. (Canceled)